REMARKS

Claims 25-37 and 39-53 remain in the application. Claims 32 and 53 have been amended. (Claim 26 is withdrawn from consideration.)

Reconsideration of the application is requested.

Formality Rejection of the Claims

In item 2 on page 2 of the above-identified Office action, claims 31-32 and 53 have been rejected as being indefinite under 35 U.S.C. § 112, second paragraph. More specifically, the Examiner stated that the feature "third power switch transistor" in claims 31 and 53 lack proper antecedent basis. The Examiner's comments have been noted and the appropriate corrections have been made to claims 31 and 53.

Prior Art Rejection of the Claims

In item 1 [sic] on page 3 of the Office action, claims 25, 27-37, 45-50, and 52-53 have been rejected as being anticipated by *Matsuzaki et al.* (US 6,500,715) under 35 U.S.C. § 102.

In items 3 and 4 on pages 5 and 7, respectively, of the Office action, claims 39-42 and claims 43-44, respectively, have been rejected as being obvious over *Matsuzaki et al.* (US 6,500,715) in view of *Sani et al.* (US 6,794,914) under 35 U.S.C. § 103.

The prior art rejections and the Examiner's comments have been considered. However, as will be explained below, it is believed that the claims were patentable over *Matsuzaki et al.* in their original form and the claims have, therefore, not been amended to overcome *Matsuzaki et al.*.

Before discussing the prior art in detail, it is believed that a brief review of the invention as claimed, would be helpful.

Claim 29 (similarly claims 51-53) recite, inter alia:

> a flip-flop having a plurality of storage transistors with a threshold voltage of a first value;

a first power switch transistor having a threshold voltage of a second value, wherein an application of a predetermined electrical potential to the first power switch transistor's gate terminal brings the circuit arrangement to an operating state in which if at least one supply voltage is switched off, electric charge carriers contained in the circuit arrangement are prevented from discharging from the circuit arrangement;

a plurality of switching transistors, having a threshold voltage of a third value, provided between the flip-flop and the first power switch transistor, for coupling a flip-flop input signal into the flip-flop wherein each of the terminals of the switching transistors has a defined electrical potential in the operating state; and

wherein the magnitude of the first and/or the second value is greater than the magnitude of the third value.

(Emphasis added.)

More specifically, the Examiner has stated that:

Figure 14 of Matsuzaki et al. shows a circuit arrangement comprising a flip flop (LH1 details shown in figure 8) having a plurality of storage transistors with a threshold voltage of a first value (high threshold), a first power switch transistor (MN1) having a second threshold voltage (high threshold), wherein an application of a predetermined electrical potential (CS) to the first power switch transistor gate terminal brings the circuit arrangement to an operating state (standby mode) in which if at least one supply voltage(VSS) is switched off, electric charge carriers (leakage current) contained in the circuit arrangement are prevented from discharged from the circuit arrangement, and a plurality of switching transistors (TP1-TP3), having a threshold voltage of a third value, provided between the flip flop and the first power switch transistor, for coupling the flip flop input signal (IN) into the flip flop, wherein the magnitude of the first and/or second value is greater that the magnitude of the third value (high threshold voltage is larger than the low threshold voltage), wherein each one of the terminals of the switching transistors (TP1 to TP3) has a defined electrical potential in the operating state (in the standby mode, the source, drain and gate terminals of the switching transistors have a defined electrical potential) [as called for in claim 29].

Matsuzaki et al. discusses the embodiment in Fig. 14 only in the last two paragraphs in col. 19, stating:

> Figs. 14-17 are examples of the case where the input IN and output OUT are different in logic level from each other during standby periods.
>
> As shown in Fig. 14, where IN and OUT differ in logic level from each other during standby periods, a switch is inserted at either IN or OUT in order to eliminate occurrence of leakage between IN and OUT. If IN="H" and OUT="L" then insert it at Vss and OUT, or at Vdd and IN. In Fig. 14 a switch MN1 is at Vss while switches MP4, MN4 are at OUT.

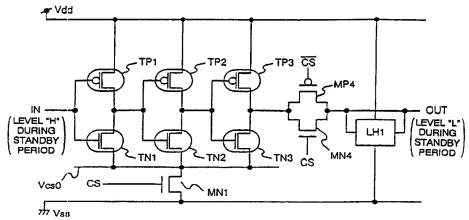
Furthermore, in col. 20, lines 47-58, *Matsuzaki et al.* states:

> It should be noted that in the above description of the embodiments, ***no particular*** limitations are given with regard to the transistor threshold value; however, it will be ***recommendable*** that the thin-film MOS transistors are of low threshold value whereas the thick-film ones are higher in threshold value than the former.

(Emphasis added.)

Fig. 14 of *Matsuzaki et al.* is reproduced below:

FIG. 14



(Note: In col. 16, lines 34-73, *Matsuzaki et al.* states "(In the transistor circuit diagrams of this application, the illustration of each thin-film MOS transistor comes with an ellipse surrounding it.).")

The Examiner did not indicate how and where the Examiner derived that *Matsuzaki et al.* discloses that the threshold voltage of the storage transistors (first value) and/or the threshold voltage of the first power switch transistor (second value) is greater that the threshold voltage of the switching transistors (third value).

As discussed in MPEP § 2112, a limitation recited in a claim that is not expressly or implicitly disclosed in a prior art reference is inherently disclosed therein if, and only if, the "missing" limitation is ***necessarily present*** in the prior art, and that it would be so ***recognized by persons of ordinary skill.*** The principles of inherency require that the inherency be ***absolute***, and not probabilistic.

As far as Applicant was able to ascertain, there is no disclosure or suggestion in *Matsuzaki et al.* that it is absolutely necessary that the threshold voltage of the storage transistors (first value) and/or the threshold voltage of the first power switch transistor (second value) is greater that the threshold voltage of the switching transistors (third value), as would be recognized by persons of ordinary skill. *Matsuzaki et al.* explicitly states that "***no particular*** limitations are given with regard to the transistor threshold value". *Matsuzaki et al.* merely states that it is "***recommendable*** that the thin-film MOS transistors are of low threshold value whereas the thick-film ones are higher in threshold value than the former." Recommendable is ***not*** necessarily. Consequently, *Matsuzaki et al.* does not disclose - whether explicitly, implicitly, or inherently - that the threshold voltage of the storage transistors (first value) and/or the threshold voltage of the first power switch transistor (second value) is greater that the threshold voltage of the switching transistors (third value).

It is accordingly believed to be clear that *Matsuzaki et al.* does not show the features of claims 29 and 51-53. Claims 29 and 51-53 are, therefore, believed to be patentable over *Matsuzaki et al.* and because claims 25-28, 30-31, 33-37, and 39-50 are ultimately dependent on claim 29, and claim 32 is dependent on claim 53, they are believed to be patentable as well.

Considering the deficiencies of the primary reference, *Matsuzaki et al.*, it is believed not to be necessary at this stage to address the secondary reference, *Sani et al.*, applied in the rejection of dependent claims 39-44, and whether or not there is sufficient suggestion or motivation with a reasonable expectation of success for modifying or combining the references as required by MPEP § 2143.

Reconsideration and allowance of claims 25-37 and 39-53 are respectfully requested.

In view of the above, Applicant believes the pending application is in condition for allowance.

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Respectfully submitted,

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